Designing an optimized half-bridge DC-DC converter with medium-voltage CoolGaN™ transistors

About this document

Scope and purpose

This application note provides detailed information on how to design a well-optimized half-bridge DC-DC converter using CoolGaN™ transistors in the 60-200 V class. This includes components selection, PCB architecture and layout, and optimization process.

Intended audience

Power electronics design engineers using low-/medium-voltage CoolGaN™ transistors.

CoolGaN™

Infineon's CoolGaN™ solution offers unmatched quality that operate at higher switching speeds resulting in lower power losses, higher efficiency paving the way for smaller and lighter power supplies with the same power supplies with the same size but increased power capability.

CoolGaN™ target applications include:

- Consumer electronics
- Information and communication technologies
- Motor drives
- Robotics
- Energy Storage Systems
- Renewables

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Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

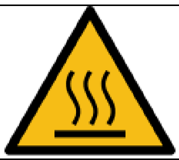
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

Table of contents

1 Introduction

This document is divided in four different sections to that will guide you to design a well-optimized half-bridge DC-DC converter using CoolGaN™ transistors in the 60-200 V class.

- Component selection **-** Each design section is corroborated with a thorough description of the component selection strategy and the formula used for the design of the component. In this way, the designer can either use the formula to complete the design or understand the reasoning behind the used formulas
- PCB architecture **-** Starts with a preliminary work, which sometimes is underestimated – strategy of the layer stack-up and board area mapping. Both phases are very important since they define the performance of the entire board (or even converter)
- PCB layout **-** Strong emphasis is given to the concept of commutation loops and the associated inductances. The reduction of those parasitic elements is vital for the correct functionality of the half-bridge, therefore numerous suggestions are provided through clear examples
- Measurement and adjustment **-** Refers to the verification through measurements of the previous parts. This section is divided in two parts. The first part offers information on the measurement techniques, which are used to verify the quality of the design and is very important since wrong measurement techniques could lead to wrong conclusions on the value of the design. The second part provides directions to select between design for performance and design for robustness

2 Step-by-step design guide for an MV CoolGaN™ half-bridge

There is no universally perfect solution as each application and each system is unique. These steps and recommendations will help to find the best fit for each design, within the constraints and available options of the project.

2.1 Component selection

The preliminary design process involves building the schematic. Figure 1 shows one example schematic using a level-shifted half-bridge gate driver, with integrated bootstrapping and split on/off outputs for each gate.

The key components include the two MV CoolGaN™ transistors, the gate driver, gate resistors, high-frequency decoupling capacitors for V_{IN} and each gate, and bulk capacitors as needed.

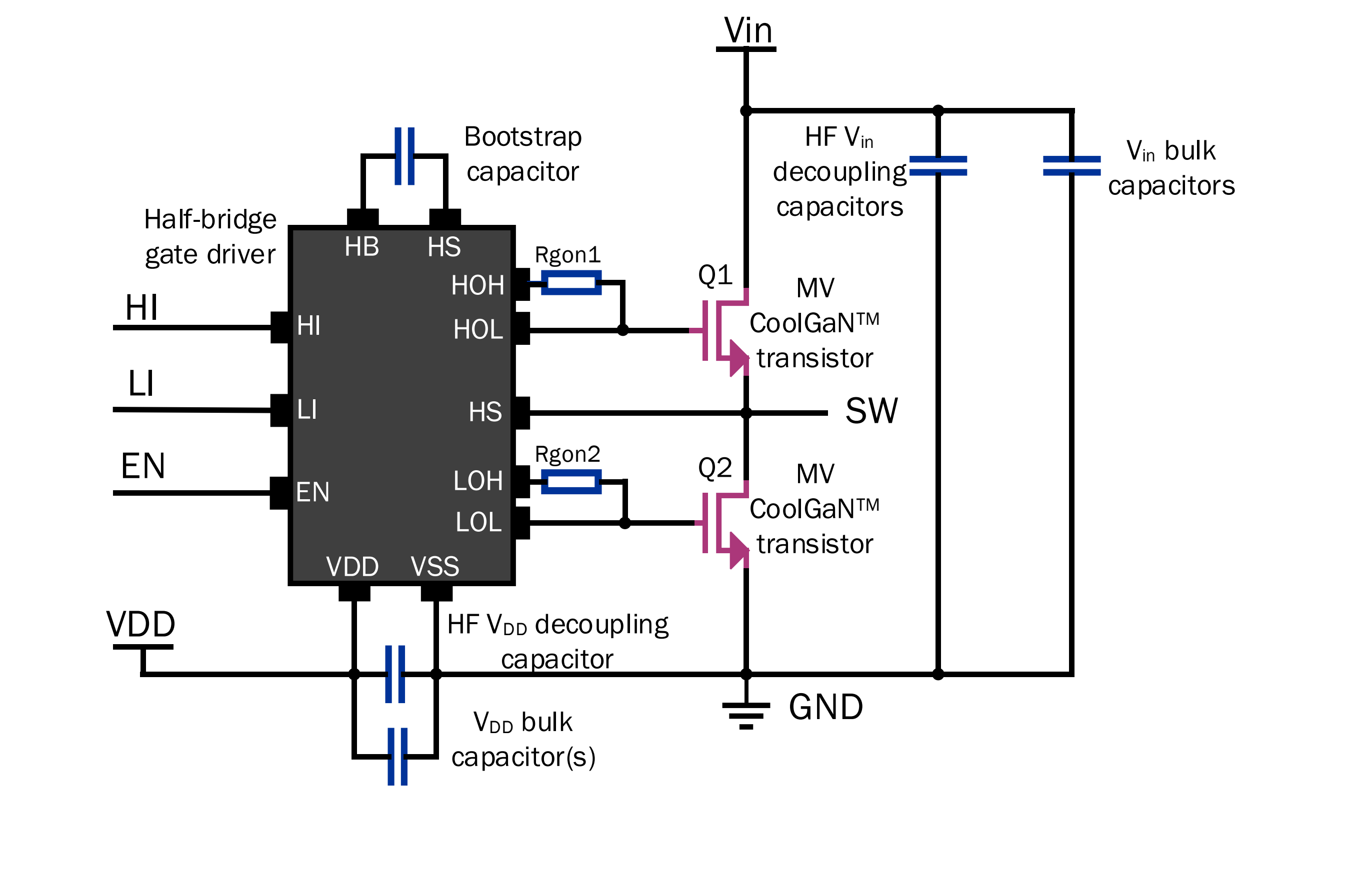


Figure 1 **MV CoolGaN™ half-bridge using a generic level-shifted half-bridge gate driver schematic**

2.1.1 CoolGaN™ transistors

Select the MV CoolGaN™ power transistor(s) for the high-side and low-side positions using the half-bridge evaluation boards such as EVAL_7136U_100V_GaNc [5]. The two 3x5 mm and 3x3 mm PQFN packages are footprint compatible and available in a range of voltage and $R_{DS(on)}$ options for different combinations in the preferred application condition.

2.1.1.1 Voltage rating

The voltage rating for the transistor is primarily based on the expected DC voltage operation and consider the switching transition overshoots. However, it is important to choose transistors such that the maximum DC operating voltage is below 80% of the rated voltage, according to JEDEC guideline JEP180 [6]. This recommendation is only for normal operating conditions and transient excursions above 80% may be acceptable. The Infineon performs detailed analysis of the application's mission profile upon request when it is expected for the DC voltage to repeatedly exceed this level. Furthermore, this does not include transient switching spikes above the DC operating point.

2.1.1.2 Channel resistance $R_{DS(ON)}$

In many applications, a symmetric half-bridge is the preferred choice, where the high-side and low-side transistors are identical. However, in applications with very steep conversion ratio or narrow duty cycle, choose different transistors for each position [7].

This depends on which device is hard-switching and which is a synchronous switch. For example, the high-side is hard-switching in a buck converter, while the low-side is a synchronous switch. In a boost converter, the roles are reversed. Motor drives and other applications with AC switch-node current do not have specified roles for each switch because the hard-switching device alternates with the current direction. In general, the hard-switching device can be identified as the transistor that conducts positive drain current and the synchronous switch conducts negative drain current.

The total power loss in a symmetric half-bridge can be estimated as:

$$P_{hb,AC} \approx {I_{SW(RMS)}}^2 R_{DS(on)} + f_{sw}\left[(t_{dt1} + t_{dt2}) I_{SW(AVG)} V_{SD} + E_{SW} + 2Q_G V_{DRV}\right]$$

Equation 1

Where,

- $I_{SW(RMS)}$ is the RMS current at the switch-node, to the filter inductor or motor phase
- $I_{SW(RMS)}$ is the time-average of the absolute value of current at the switch-node
- $R_{DS(on)}$ is the on-resistance of the switches, taking junction temperature into account
- f_{SW} is the switching frequency
- t_{dt1} and t_{dt2} are the dead-times of each switching edge per cycle
- V_{SD} is the Diode Like Behavior specified in the transistor datasheet
- Q_G is the total gate charge between the off-state voltage and on-state voltage (typically 0~5 V)
- V_{DRV} is the driving voltage swing from off-state to on-state (typically 0~5 V)
- E_{SW} is the switching energy dissipated by the hard-switching transistor per cycle

This switching energy is composed of two parts — turn-on loss and turn-off loss. However, the turn-off loss is typically negligible compared to the turn-on component. Therefore, in fully hard-switching applications, E_{SW} can be estimated as:

$$E_{SW} \approx V_{IN} Q_{OSS2} - E_{OSS2} + E_{OSS1} + \frac{1}{2} t_{SW,on} V_{IN} I_{OUT(AVG)}$$

Equation 2

Where,

- V_{IN} is the dc operating voltage of the half-bridge
- Q_{OSS2} is the output charge of the synchronous switch, calculated at the specific V_{IN}
- E_{OSS1} and E_{OSS2} are the output energies of the hard-switching device and synchronous switch, respectively
- $t_{SW,on}$ is the duration of the turn-on transition

Consider the complete turn-on transition time and not the simplified 90% to 10% rise/fall time of the waveform. The overlap loss occurs throughout the entire voltage transition, including the nonlinear portions at the start and end, which is often much longer than the 90% to 10% value.

The duration of this transition is not easily estimated before beginning the design, as this is typically a design choice based on V_{DS} overshoot and slew rate. With a suitably strong driver, the transition time can be less than 3 ns but this may not meet the system requirements for overshoot or slew rate.

In the case of a motor drive phase leg, the loss of the half-bridge is equally distributed between the two transistors. However, in most other applications, one transistor experiences the full hard-switching loss, while the other experiences the full dead-time conduction loss. In such a case, the loss in each transistor can be estimated as:

$$P_{Q1} \approx {I_{SW(RMS)}}^2\, D\, R_{DS(on)1} + f_{sw}[E_{SW} + Q_{G1}V_{DRV}]$$

Equation 3

$$P_{Q2} \approx {I_{SW(RMS)}}^2(1-D)R_{DS(on)2} + f_{sw}\left[(t_{dt1} + t_{dt2})I_{SW(AVG)}V_{SD2} + Q_{G2}V_{DRV}\right]$$

Equation 4

Where, Q1 is assumed to be the hard-switching transistor and Q2 is assumed to be the synchronous switch and D is the duty cycle/ratio of Q1 on-time.

These equations are useful in preliminary estimations of loss and selection of MV CoolGaN™ transistors.

2.1.2 Gate driver ICs and gate resistors

MV CoolGaN™ transistors have a Schottky-type gate, which emulates a MOSFET gate in many ways. The gate is not truly insulated however, the leakage current is low enough that it can be mostly ignored in the design of the driving circuit. The gate driver IC (GDIC) can therefore, be a conventional MOSFET driver, with some special requirements ([4], [8], and [9]):

- Compatibility with the necessary driving voltage, typically 5 V with a UVLO sufficiently below that level
- Low-inductance package with pinouts fitting well to an optimized PCB layout, while also maintaining the required clearance values for the application. For example, a ball grid array wafer-level chip-scale package (BGA WLCSP) may offer the lowest inductances but it may not be easily compatible with assembly on a high-power PCB with thick copper, risking low board yield or creepage-related arcs between bumps
- Compatibility with the target dv/dt for the high-side switch, often defined as common-mode transient immunity (CMTI) for an isolated GDIC
- Sufficiently low pull-up and pull-down resistances to achieve the desired performance, as well as peak source and sink currents

- For level-shifted half-bridge GDICs, the level-shifting circuit must be fully operational when the switching node voltage dips to the highest DLB voltage of the GaN transistors, typically in the range of -3 to -5 V when the off-state gate voltage is 0 V
- For GDICs with bootstrapping features, some regulation must be employed to maintain the bootstrap voltage near the GDIC supply voltage (e.g., 5 V), especially during dead-time Diode Like Behavior conduction. In some cases, a Zener-based regulation scheme can be employed when the driving IC does not offer this feature
- In scenarios where the PCB layout cannot be well-optimized, a negative off-state voltage may be required to avoid Miller-induced turn-on during hard-switching transitions. However, negative voltage will impact the performance due to the increase of the dead-time losses
- For added value, it is helpful for the GDIC to offer an unpowered gate clamp, pulling the gates low when the supply voltage is not present or not high enough to power on the driver. Otherwise, a resistor may be needed between each gate and source terminal
- The turn-on and turn-off external gate resistors control the turn-on and turn-off current of the gate driver, providing an external way to control the switching speed of the MOSFET for purposes such as voltage overshoot control, ringing reduction, EMI mitigation, spurious turn-on protection, shoot-through protection, etc
- If the GDIC produced the desired switching transition without external gate resistors, then none should be used. However, many drivers offer a higher peak source current and lower pull-up resistance than the designers prefer, in which case an external gate resistor may be used. In most well-optimized designs, a turn-off gate resistor in series with the OUTSNK pin is not recommended, as this may block the GDIC from mitigating the Miller effect and lead to induced turn-on
- When selecting the gate resistor value, consider its value relative to the internal resistance inside the GaN transistor as well as the pull-up or pull-down of the GDIC. The following formulas show how these different resistances result in the effective peak output current of the gate driver, often lower than the specified value in the driver datasheet

$$I_{SRC,PK} \leq \frac{V_{DD}}{R_{PU}+R_{G,int}+R_{Gon,ext}}$$

Equation 5

$$I_{SNK,PK} \leq \frac{V_{DD}}{R_{PD}+R_{G,int}+R_{Goff,ext}}$$

Equation 6

Where,

- $I_{SRC,PK}$ = Peak source current
- $I_{SNK,PK}$ = Peak sink current
- R_{PU} = Gate driver pull-up resistance
- R_{PD} = Gate driver pull-down resistance
- V_{DD} = Gate driver supply voltage (equivalent to VBOOT for high-side transistor)
- $R_{G,int}$ = Internal gate resistance of driven transistor
- $R_{Gon,ext}$ = External gate resistance connected between Source output and gate
- $R_{Goff,ext}$ = External gate resistance connected between Sink output and gate (not typically recommended)

The selected value for $R_{Gon,ext}$ has a strong impact on the switching waveforms and system performance

2.1.3 Bootstrap diode and regulation circuit

In half-bridge topologies, a bootstrapping circuit is often used to supply the high-side driver's V_{DD} ([8] and [9]). If the GDIC does not include an integrated bootstrap diode or active bootstrap switch, add an external diode. A fast recovery or Schottky diode with low forward voltage drop is recommended to minimize the losses and leakage current. It should be chosen such that it can handle the peak transient current during start-up conditions and the blocking voltage rating should be higher than the maximum input voltage (V_{IN}) with added margin. It is important to consider that the output capacitance and reverse recovery of this bootstrap diode contributes to the total switch-node capacitance of the half-bridge, thereby increasing the total switching losses of the application circuit. A Schottky diode with low output capacitance is therefore, preferred for most applications.

Many GDICs offer some type of bootstrap voltage regulation, such as the EiceDRIVER™ 1EDN71x7x family. When no regulation is employed, a conventional Zener-based regulation scheme can be used ([8] and [9]).

2.1.4 Gate loop decoupling capacitors

The GDIC VDD bypass capacitor provides the gate charge to drive the low-side transistor, as well as additional power consumption by the IC itself. It should be placed as close as possible to the V_{DD} and V_{SS} pins of the gate driver, which may require a particular footprint size for most applications.

The minimum value for this bypass capacitor can be calculated based on the maximum allowable voltage ripple in the design. This ripple should be minimized such that the lowest possible V_{DD} is above the UVLO limit of the gate driver as well as above the safe driving voltage of the transistor. The charge dissipated per switching event is approximately equal to the driven transistor's gate charge. The minimum value can therefore, be calculated as:

$$C_{Vdd} \gg \frac{Q_G}{\Delta V_{DD,max}}$$

Equation 7

In a half-bridge configuration, the V_{DD} bypass capacitor also provides the charge for the bootstrap capacitor during the charging period. Therefore, ensure that the V_{DD} bypass capacitor’s size is larger than the bootstrap capacitor. The minimum value should be calculated as:

$$C_{Vdd} \gg \frac{Q_G + Q_{BOOT}}{\Delta V_{DD,max}}$$

Equation 8

Where,

QBOOT is the charge consumed by the bootstrapping circuit each cycle.

The bootstrap capacitor provides the necessary charge to drive the high-side transistor. Ensure that its sized in such a way that its lowest voltage will be much higher than the UVLO threshold as well as above the minimum safe driving voltage of the transistor, during transient and normal operations.

To determine the minimum required bootstrap capacitance, the maximum allowable ripple in VBOOT must be calculated as:

$$\Delta V_{BOOT,max} = V_{DD} - V_F - V_{BOOT,min}$$

Equation 9

Where,

- V_{DD} = Low-side gate driver supply voltage
- V_F = Bootstrap diode forward voltage drop

$V_{BOOT,min}$ is the minimum allowable voltage for the bootstrap capacitor, including transient events. This voltage must be at least high enough to avoid UVLO shutdown, as given by:

$$V_{BOOT,min} \geq V_{HBR} + V_{HBH}$$

Equation 10

Where,

- V_{HBR} = High-side driver UVLO rising threshold
- V_{HBH} = High-side driver UVLO threshold hysteresis

However, the driven transistor may require a higher voltage than this UVLO minimum to remain fully on and avoid linear-mode operation. If the calculated minimum VBOOT is lower than the safe driving voltage of the transistor, then $V_{BOOT,min}$ should be increased accordingly.

Additionally, the total charge (QBOOT) that must be delivered by the bootstrap capacitor at maximum duty cycle should be determined. There are several factors that contribute to the discharge of the bootstrap capacitor such as the high-side transistor's total gate charge and gate-source leakage current, bootstrap diode reverse bias leakage current, and bootstrap capacitor leakage current. However, the bootstrap capacitor leakage current can typically be neglected.

The total bootstrap charge can be estimated as:

$$Q_{BOOT} \approx Q_G + \frac{I_{Vdd} + (I_{diode} \times D_{max})}{f_{sw}}$$

Equation 11

Where,

- Q_G = High-side transistor total gate charge
- I_{Vdd} = High-side driver maximum quiescent current
- I_{diode} = Bootstrap diode reverse bias leakage current
- D_{max} = Maximum high-side duty cycle
- f_{sw} = Switching frequency

The minimum bootstrap capacitor value can then be calculated using the formula:

$$C_{BOOT} \gg \frac{Q_{BOOT}}{\Delta V_{BOOT,max}}$$

Equation 12

In practice, these capacitance values should be significantly increased to account for DC bias effects in the capacitor and other non-idealities in the circuit, typically by a factor of 2~10. When scaling up these capacitance values, it is important to consider the tradeoff between system stability and the necessary charging time during system startup. Higher capacitance values will help support transient operation with very short duty cycles but lower values will enable a faster system startup.

Place a small resistor between the local V_{DD} of the half-bridge circuit and the global V_{DD} rail supplying it to limit the inrush current during startup and avoid high-frequency interaction between different circuits utilizing that rail. Similarly, place a resistor in series with the bootstrap diode to limit the inrush when starting up the bootstrap circuit. However, exercise caution during the placement of these resistors. If the resistor is placed between the decoupling capacitor and the GDIC, it acts as an additional $R_{Gon,ext}$ as explained in Section 2.1.2 and it may risk UVLO events during transient application conditions.

2.1.5 Power loop decoupling capacitors

Place the high-frequency decoupling capacitors for the V_{IN} rail (high-side drain) locally to define the power loop (Section 2.3.1). These capacitors can be very low in value if larger bulk capacitors are placed elsewhere in the design to maintain a stable voltage.

When selecting the capacitance value, consider the potential droop in local V_{IN} with each switching transition caused by the loss of E_{SW} in each cycle as explained in Section 2.1.1. When the GaN transistors dissipate this energy each cycle, replenish the decoupling capacitors by the bulk capacitors for a momentary drop in voltage, that will result in some ringing between the two capacitor banks. The amplitude of this ringing and the value of the voltage droop can be estimated as:

$$\Delta V \approx \frac{E_{SW}}{C_{decoupling} V_{IN}}$$

Equation 13

The minimum value for the decoupling capacitor bank can therefore, be selected based on the selected value *k*, the percentage of droop relative to the nominal dc voltage on that rail (e.g., 1%):

$$C_{decoupling} > \frac{E_{SW}}{k\, V_{IN}{}^2}$$

Equation 14

Consider the following two parameters:

- The effective capacitance value using the manufacturer guidance on the DC bias effects at the nominal operating voltage of the V_{IN} rail
- The equivalent series inductance (ESL) of the capacitors
  However, this is typically constant for a given aspect ratio of multi-layer ceramic capacitor (MLCC). The best way to minimize ESL is to use several capacitors in a row. For example, if the minimum required decoupling capacitance is estimated as 100 nF, a row of five 20 nF capacitors in 0603 footprint would have lower ESL than a single 100 nF 0805 capacitor. In some cases, using the highest value in a given footprint gives the

opportunity to reduce the required bulk capacitance elsewhere in the system, achieving higher power density and reducing BOM cost

2.2 PCB architecture

This section discusses the PCB architecture including the layer stack-up and designation of areas of the board for specific purposes.

2.2.1 Layer stack-up

PCB layer stack-up is one of the most critical design choices in a well-optimized GaN design as all further decisions hinge on this foundation.

PCB stack-ups are grouped into two categories:

- **Equal layer spacing throughout:** The equal layer stack-up is not preferred in a GaN design as it can be difficult to manage the tradeoff between loop inductances and parallel plate capacitance
- **Differential pairs:** A differential pair stack-up uses alternating thick and thin cores/prepregs so that each layer is paired with exactly one closely-spaced layer, while the gap to its other adjacent layer is much wider, which makes it the ideal choice for a GaN design as shown in Figure 2.

The simplest version of a differential pair stack-up is the four-layer PCB shown in Figure 2; "(a)", with one thick core in the center and thinner prepregs beneath the outermost copper layers. This approach can be applied with more layers as shown in Figure 2 "(b)" and "(c)".

In a system design with noisy switching circuits on one side (e.g., top layer) and sensitive control/communication circuits on the other side (e.g., bottom layer), it may be useful to apply a stack-up as shown in Figure 2 "(d)". Here, four layers can be designated for switching circuits while four layers are dedicated to control/communication, and each half of the stack-up has its own blind via type that can be used independently of the other half.

The dielectric thickness below the outermost two layers is critical. One or both sides of the board have power transistors and/or gate drivers, as well as the associated decoupling capacitors to define the switching loops (Section 2.3). It is a prerequisite that the outer layer has a closely spaces first inner layer to close the loop and cancel the magnetic field directly below the outer layer copper. Depending on the copper thickness and manufacturing design rules, it may be possible to reduce this spacing to 50~120 µm. With an outer copper weight of 70 µm (2 oz.), a thickness of 80 µm is preferred.

The differential layers can be used for shielding or for extra parallel current-carrying copper. The thick dielectric on either side of the pair limits the parallel plate capacitance across that dielectric, providing more flexibility to the designer in making these designations.

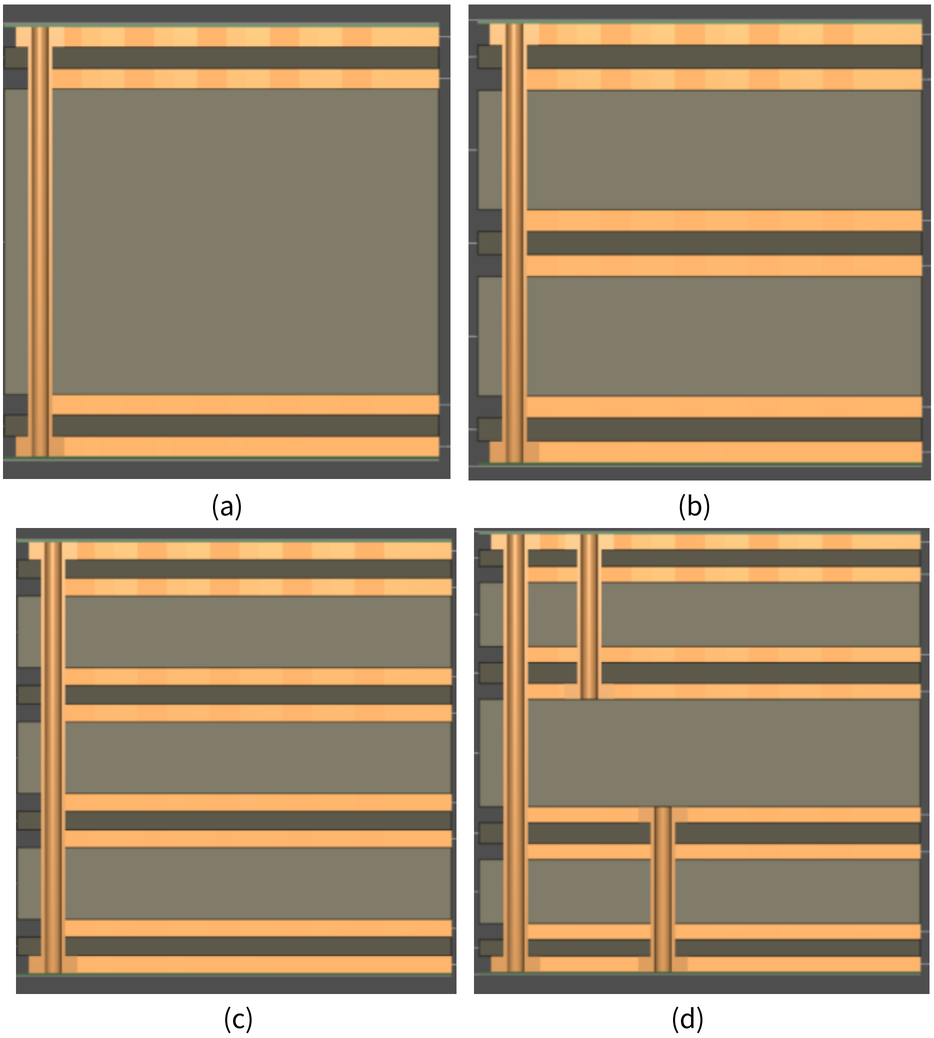


Figure 2 **(a) 4-layer stack-up; (b) 6-layer stack-up; (c) 8-layer stack-up with only through-hole vias; (d) 8-layer stack-up with through-hole and blind vias**

2.2.2 Board area mapping

Broad area mapping includes the positions of connectors (input power, output power, control/communication interfaces) as well as the half-bridges and other functional blocks of the system schematic. Map out these areas before beginning the actual layout process to avoid parallel plate capacitance issues and signal coupling glitches.

The half-bridge layout technique shown in Section 2.3 aims to keep the switching loop small to minimize inductance and avoid coupling noise into other circuits of the board. Stray capacitance between the switching-nodes and DC circuits create parallel switching loops, experiencing the same dv/dt as the transistors themselves. These parallel switching loops may travel much further around the board and cause persistent or intermittent malfunctions. Therefore, localize any switch-node capacitance to the area and layers of the half-bridge and its intentional switching loops.

2.3 PCB layout

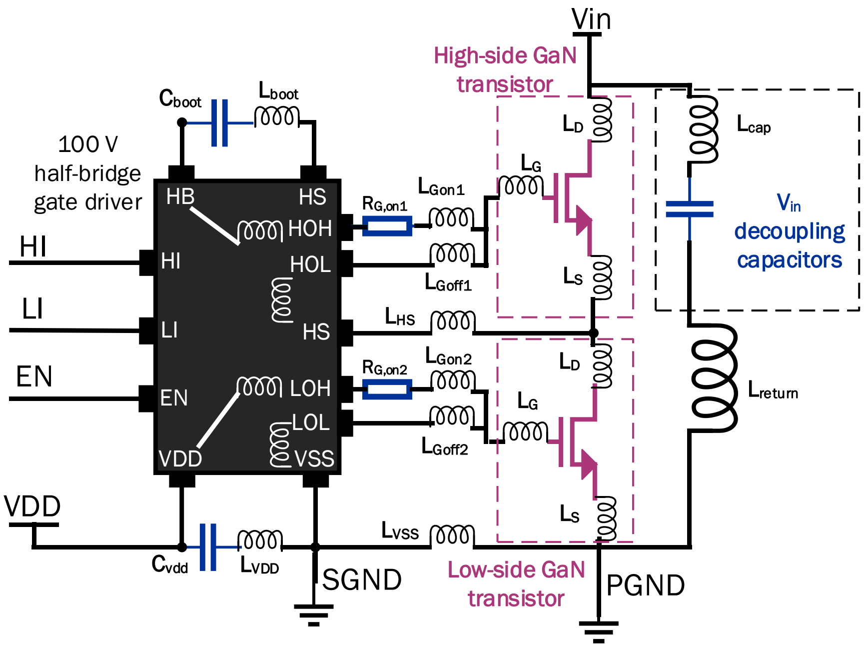
This section provides recommendations for critical switching circuits in the half-bridge, including the impact factors of stray inductance in each loop, and guidelines for minimizing them.

2.3.1 Overview of switching commutation loops

The primary goal of the MV CoolGaN™ half-bridge layout is to minimize the switching commutation loops. These loops contain the inductances that result in drain voltage overshoot, gate voltage overshoot, and spurious switching events. In Figure 3 "(a)" indicates some of the lumped inductances within the components and between them, while "(b)" highlights the displacement current paths involved in turn-on and turn-off transitions.

Whenever the drain voltage swings to V_{IN} or PGND, charges must be displaced between $C_{OSS,Q1}$ and $C_{OSS,Q2}$, as one V_{DS} rises and the other falls. The displacement current follows the path marked with a blue arrow, flowing between the two transistors and the nearest V_{IN} decoupling capacitors. MV CoolGaN™ transistors come in an ultra-low-inductance package, meaning that the dominant inductances in this loop come from the decoupling capacitors and the return loop that connects the components together.

Similar loops are followed whenever a gate voltage rises to turn on the transistor marked with yellow arrows in the figure. However, when the gate voltage is falling to turn off a transistor, this loop is slightly different. During a gate turn-off, the gate charge Q_G is removed from the gate and dissipated passively as by the driver IC. Therefore, the turn-off gate loop does not contain any capacitors, as shown with orange arrows. In a turn-on transition, the driver moves charge into the gate, so this loop must contain a capacitor to supply the charge.



(a)

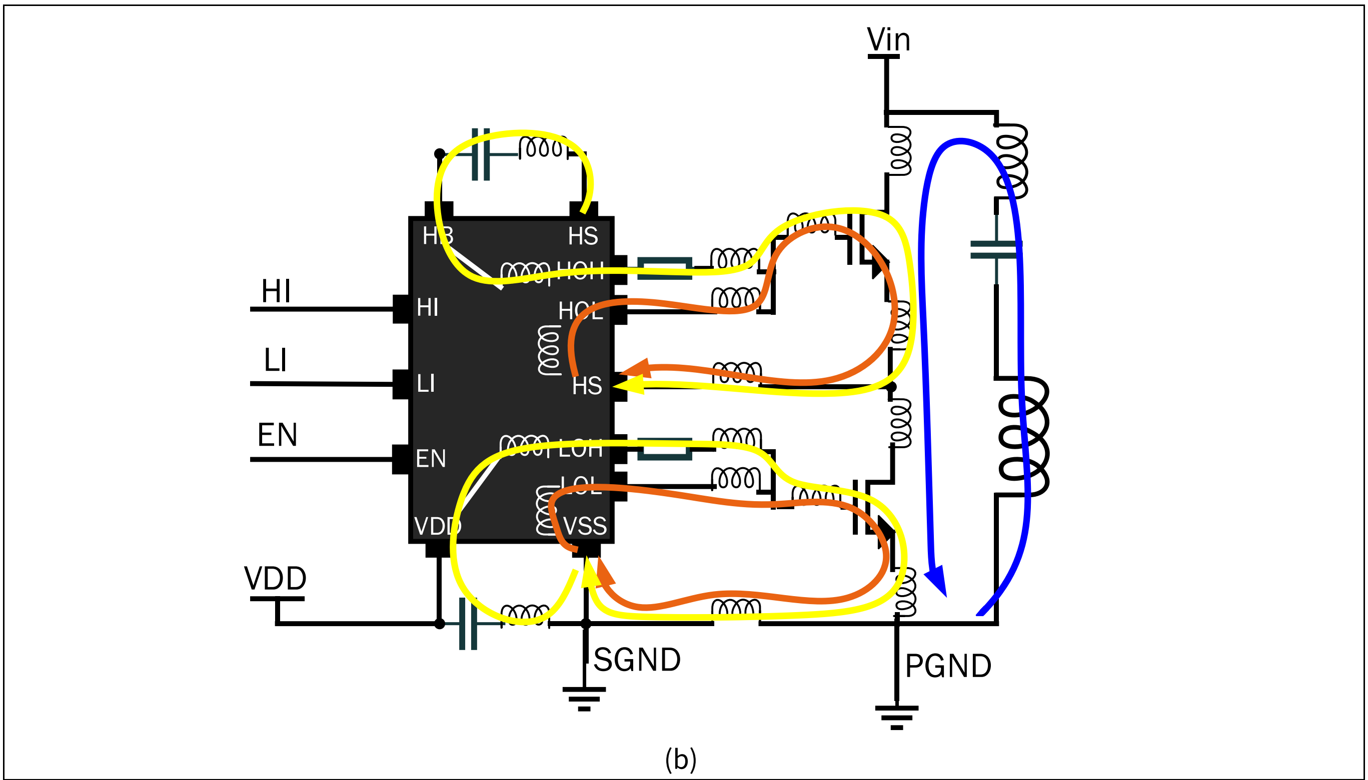


Figure 3 **Simplified representation of a GaN half-bridge circuit with a generic half-bridge gate driver, (a) annotated with the parasitic inductances inserted into power loop and gate loops; (b) with the power loop indicated in blue, turn-on (source) gate loops indicated**

The power loop is mostly independent of the gate loops. However, it is clear from Figure 3 that the inductances labeled "LS" are shared between the power loop and gate loops. This common-source inductance can be very small but can become problematic if not managed well. A high common-source inductance generally has the same effect as a large gate resistor, slowing down the turn-on and turn-off transitions and causing additional switching loss.

2.3.2 Minimizing loop inductances with first inner layer return

The "first inner layer return" PCB layout technique uses magnetic field cancellation to minimize all of the inductances shown in Figure 3 while also containing the high-frequency current to a tight area to limit unwanted coupling ([1], [2], and [4]).

Figure 4 and Figure 5 show examples of this layout implemented with a level-shifted half-bridge gate driver and with single-channel high-side drivers, respectively. The green arrows indicate half of each loop shown in Figure 3 and the red arrows show the other half of each loop.

Each loop is split between the top copper layer and first inner layer with vias located to allow for the current path on the inner layer to mirror the path on the top. The shielding polygons on this inner layer are sometimes described as "image planes", where the current path of the top layer is projected down to the polygon below even if there are more direct routes for the current to flow between vias on the inner layer.

Furthermore, consider the separation of the power loop and gate loops to limit common-source inductance and avoid unwanted side-effects that might result from it. This separation can be accomplished in several ways: The gate loops can be routed perpendicular to the power loop, whenever possible as shown in Figure 5 (the geometrical approach) or provide a separate PGND island for the low-side gate return.

The geometrical approach is more difficult with half-bridge drivers, where the gate loop must run somewhat in parallel to the power loop due to the position of the driver. In Figure 1, a vertical slit is cut out from the PGND polygon to separate the gate and power loop returns only in the area where the two loops run nearly parallel. It is optional to completely island this gate shield or to navigate the issue with careful use of geometry and cutouts. Either approach will ensure low common-source inductance for the low-side gate loop where it flows on mid-layer 1.

With proper implementation of the technique, the connections of gate loops and power loops on other PCB layers are less critical. Any commutation loops beyond the first inner layer are in parallel to the lowest inductance/impedance path and therefore, will conduct very little switching current. In the same way, it is fine to allow lateral power loops or gate loops to be present on the top layer. As long as there exists a lower-inductance path in parallel with the first inner layer return, these other loops will only support with the conduction of low-frequency power currents and not play a major role in the switching commutations. This is especially helpful for routing the first source pad, the shortest source pad positioned next to the gate. MV CoolGaN™ does not require a Kelvin source because the inductances inside the package are low. However, this first source pad is mainly used as a gate loop return on the first inner layer. On the top layer and all other layers, the pad and its related vias can be connected elsewhere for power flow. This approach mitigates common-source inductance without cutting off that source pad from the flow of steady-state current.

Additionally, the placement and types of vias are also important considerations. When possible, vias-in-pad are an excellent way to shrink commutation loops and also conduct heat and power to large copper polygons on other layers of the PCB. When within a pad, fill the via with conductive material or non-conductive epoxy to prevent solder paste from leaking through. This manufacturing process is more expensive than standard vias. Therefore, when filled vias are too costly, it is reasonable to place the vias nearby to the components without being directly within the pads. This increase the inductance in critical loops but it may be an acceptable compromise when unavoidable. When vias cannot be placed in pads, increase the distance between the high-side and low-side transistors to allow an open alley for phase-node current to travel to the load and also for a less congested heat gradient around each transistor.

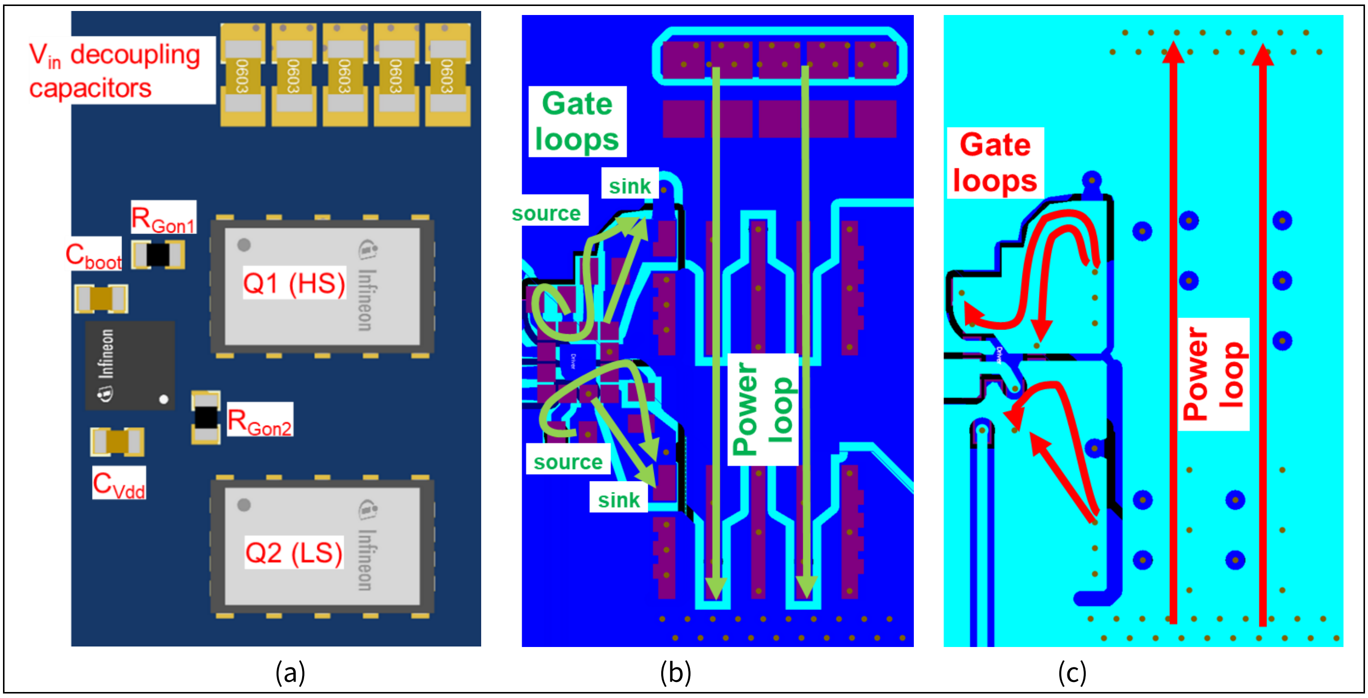


Figure 4 **Half-bridge layout for CoolGaN™ in 3x5 mm PQFN package, using a generic half-bridge gate driver; (a) Top view of board; (b) Top copper layer with components pads marked in purpose and displacement loop positive paths marked in green; (c) Mid-layer**

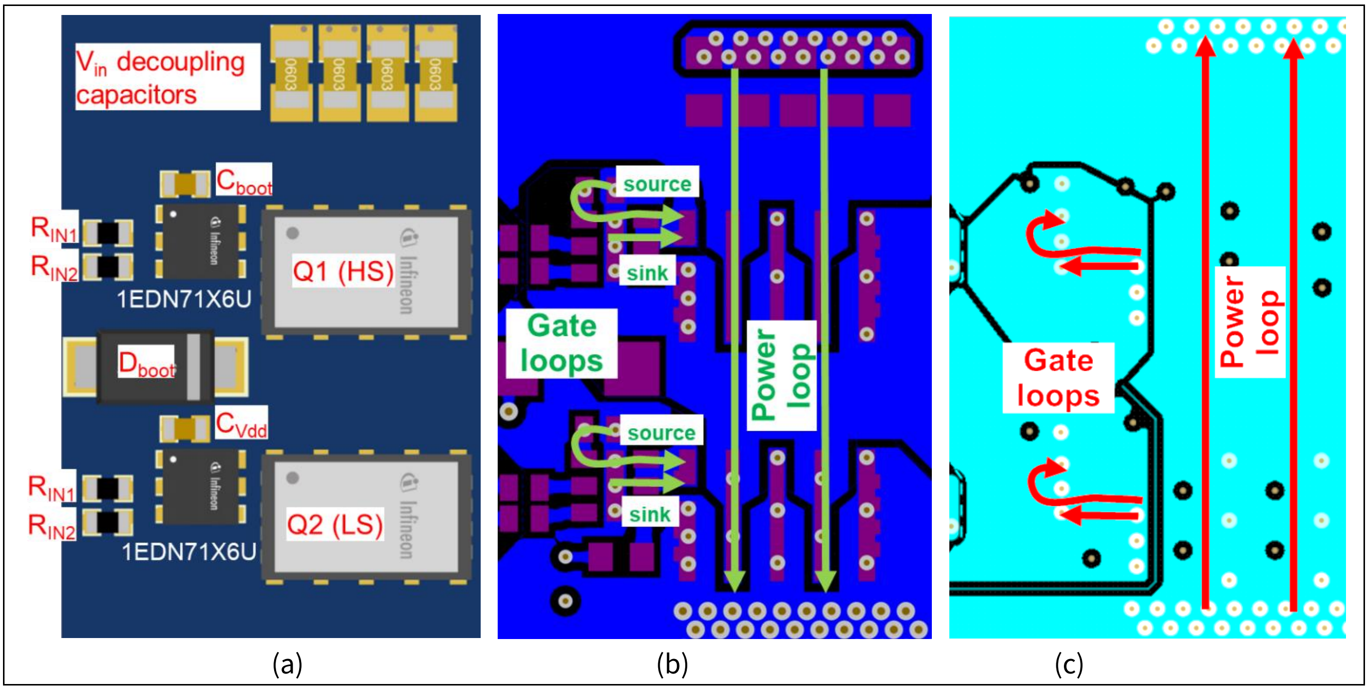


Figure 5 **Half-bridge layout for CoolGaN™ in 3x5 mm PQFN package, using single-channel TDI gate drivers from the EiceDriver™ 1EDN71x6U family; (a) Top view of board; (b) Top copper layer, with components pads marked in purpose and displacement loop positive paths marked in green; (c) Mid-layer 1, with displacement loop return paths marked in red**

When vias-in-pad are used, avoid the "Swiss cheese effect" that occurs when the first inner layer is interrupted by too many via holes. For example, in Figure 4 and Figure 5, the first inner layer return is used for the PGND net on the low-side source. However, there are several switch-node vias beneath the low-side and high-side transistors and these vias create gaps in the PGND return on the first inner layer. As long as there is significant copper below the transistors for the return current to flow, this usually causes minimal increase in the loop inductance. To mitigate the "Swiss cheese effect", use the "Remove unused pad shapes" tool in the PCB design software to eliminate the annular rings around vias on layers where they do not connect to other objects. This tool allows for the polygons to repour closer to the via hole.

There are instances where the gate drivers cannot fit on the same side of the PCB as the transistors due to space constraints. Locate the driver on the opposite side of the board using this same approach. The gate loop inductances will be higher but proper shielding has a significant impact. Ensure that the entire driving circuit is on the side with the driver, especially the low-side and high-side decoupling capacitors. The gate resistor can optionally be next to the driver or next to the transistor's gate pad. In this case, position the gate shielding islands in the inner layer below the driving circuit rather than below the transistors.

2.3.3 Power loop layout options

The first inner layer return is a basic framework for half-bridge layout. This section shows some variations of the implementations in Figure 4 and Figure 5 that can work well, and explain why some variations are not recommended.

Figure 6 shows three options for an optimal return for the power loop, while the gate driving circuit layout remains similar to the previous section.

- Part "(a)" is the same layout as shown in Figure 4 and Figure 5, where the PGND net (low-side source) is used to close the power loop on the first inner layer

- Part "(b)" repositions the decoupling capacitors near the low-side source and uses the V_{IN} net (high-side drain) to close the loop
- Part "(c)" moves the capacitors between the two transistors, and here the switch-node is used as the loop return

All three of these options result in the same cross-sectional loop area depicted in part "(d)".

The low inductance comes from the tight spacing between these two layers, the length of the path on both layers and the width of the loop (i.e., the number of parallel arrows that can be drawn in the diagram). For example, with 80 µm dielectric thickness, the cross-sectional area is ~1 mm², the width is ~4 mm, and the loop inductance is ~400 pH.

Figure 7 shows two commonly implemented alternatives, (a), the vertical two-sided loop and (b), the lateral loop. These two half-bridges result in significantly higher power loop inductance. The path length for the vertical loop looks shorter but the loop area now crosses the full thickness of the PCB. With a 1.4 mm thick PCB, the cross-sectional area is now 4 mm² for the tightest loop, and 13 mm² for the widest loop. The lateral loop has a similar issue. The tightest loop is only 2 mm² in area, while the widest loop is 30 mm². The high-frequency displacement current is likely to favor the smaller 2 mm² loop area meaning that the loop width is very small, likely <1 mm. Both of these layouts exceed 1 nH in power loop inductance. Furthermore, it is more challenging to geometrically decouple the gate loops from the power loop in the lateral implementation.

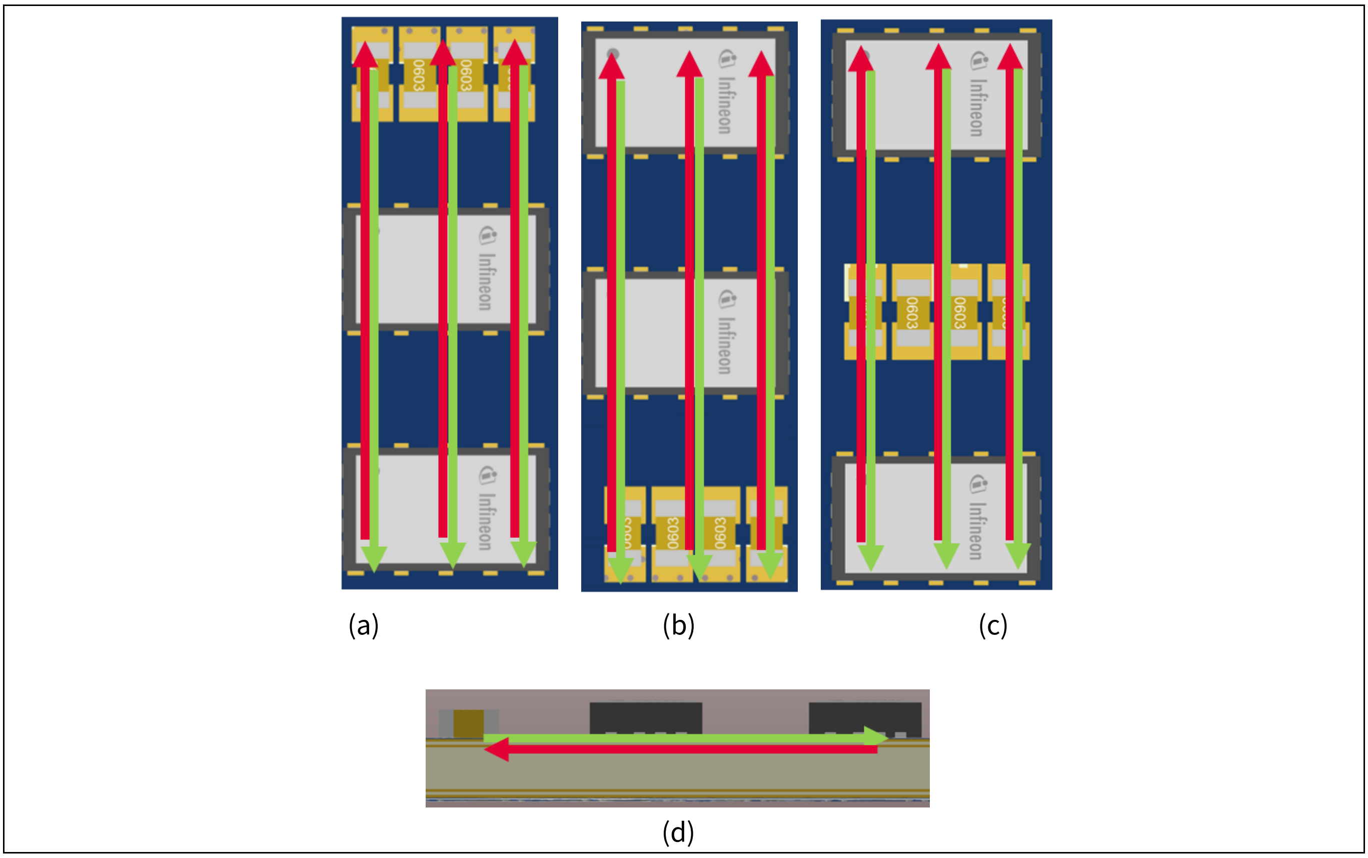


Figure 6 **Recommended half-bridge layout for MV CoolGaN™ in 3x5 mm PQFN package showing three options for first-inner-layer return. (a) GND return; (b) VIN return; (c) SW return; (d) cross-sectional view of GND return to visualize the loop area**

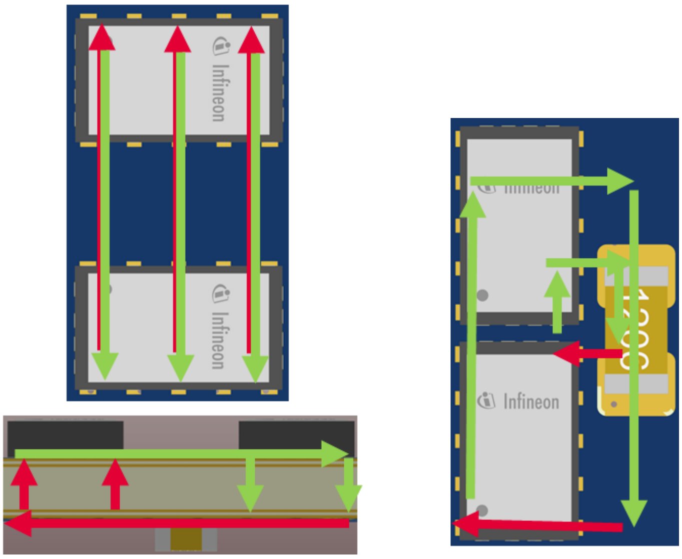


Figure 7 **Non-optimal half-bridge layouts for MV CoolGaN™. (a) Vertical loop with capacitors on opposite side of PCB, top view and cross-sectional view; (b) Lateral loop with return on same layer as components**

2.4 Measurement and adjustment

Once the design has been reviewed and built, the final step is to perform the measurements and fine-tune a few remaining parameters.

2.4.1 Waveform measurements

In Section 2.1, the gate driving strength and turn-on gate resistors were selected without clear constraints on the switching speed. At this point in the design process, these choices can be reconsidered to adjust the turn-on transitions to fit the project requirements. In most cases, the first constraint to consider is the drain voltage overshoot. When one switch turns on with positive current flow into the drain (i.e., a hard turn-on), the complementary switch experiences a sudden rise in its V_{DS}. This rise rate and the resulting ringing are consequences of the gate driving strength and value for $R_{G,on}$. A higher resistor value will slow down the slew rate and reduce the overshoot, as well as the amplitude of the ringing that follow the transition.

It is important to measure these waveforms as accurately as possible. Refer to [11], [12], and [13] for recommendations on measuring waveforms of GaN and other fast-switching transistors. Important considerations include the bandwidth and sampling rate of the oscilloscope, as well as the bandwidth and connectivity of the probe. MV CoolGaN™ waveforms can typically be captured accurately using a probe and oscilloscope with bandwidths of 1 GHz or more, although lower values may be acceptable for relatively slow transitions. Similarly, a sampling rate of 10 GHz (10 Gigasamples per second) is a good value to capture an accurate waveform, with lower values sometimes sufficient.

In the case of high-side probing, the common-mode rejection ratio (CMRR) is crucial to an accurate measurement, usually requiring fiber optical isolation. Example probing solutions include the Tektronix TPP1000 or PMK MMCX series for low-side measurements, and Tektronix isoVu or PMK Firefly for high-side measurements. Example oscilloscope options include the Tektronix MSO 5-series or Keysight MXR series.

Even the most advanced measuring system requires careful attention to the probe tip connectivity, which includes the physical connection of the probe tip to the PCB, as well as the internal routing of the PCB from the tip connection to the actual pads of the GaN transistor.

Figure 8 demonstrates some examples of probe tip connectivity as provided for half-bridge evaluation board EVAL_7136U_100V_GaNc [5]. Figure 9 shows example waveforms collected on the same board.

- The low-side measurements are collected using Tektronix TPP1000 passive probes, with the screw-on MMCX tip adapter in one case or with the needle tip and “spring clip” for grounding in the other two cases
- The high-side measurements are collected using the Firefly probe from PMK, where only the recommended MMCX tip option is shown
- The three low-side V_{DS} waveforms were collected simultaneously for the same switching transition, but the peak overshoot voltages are visibly different between the three

This demonstrates the sensitivity of the measurement to probe tip connectivity. Differential PCB routing from the device pads to the tip connector helps to mitigate adverse effects however, there is some distortion of the signal as the distance is increased beyond a few millimeters, often resulting in an exaggerated peak voltage and sometimes additional ringing artifacts (i.e., “blips”) in the waveform. Similar distortion occurs with the wider measurement loop introduced by the “spring clip” grounding lead or with a twisted-pair flywire connection to reach tight spots in the board. In most application boards, there is no practical way to implement a perfect waveform measurement. The examples shown in Figure 8 and Figure 9 provide guidance for a reasonably effective probe connection.

Using these waveform results, the gate resistors or driving strength can be adjusted to suit the design targets, whether that is peak overshoot amplitude or slew rate. Multiple test conditions should be evaluated for the most effective selection, such as minimum and maximum input voltage, duty cycle, load current, and temperature. If multiple switching frequencies are under consideration, this may also be a factor in the waveform shape. In the case where the switch-node current changes polarity over a fundamental cycle, e.g., motor drives, it is also important to inspect the voltage rise and fall transitions with both current directions.

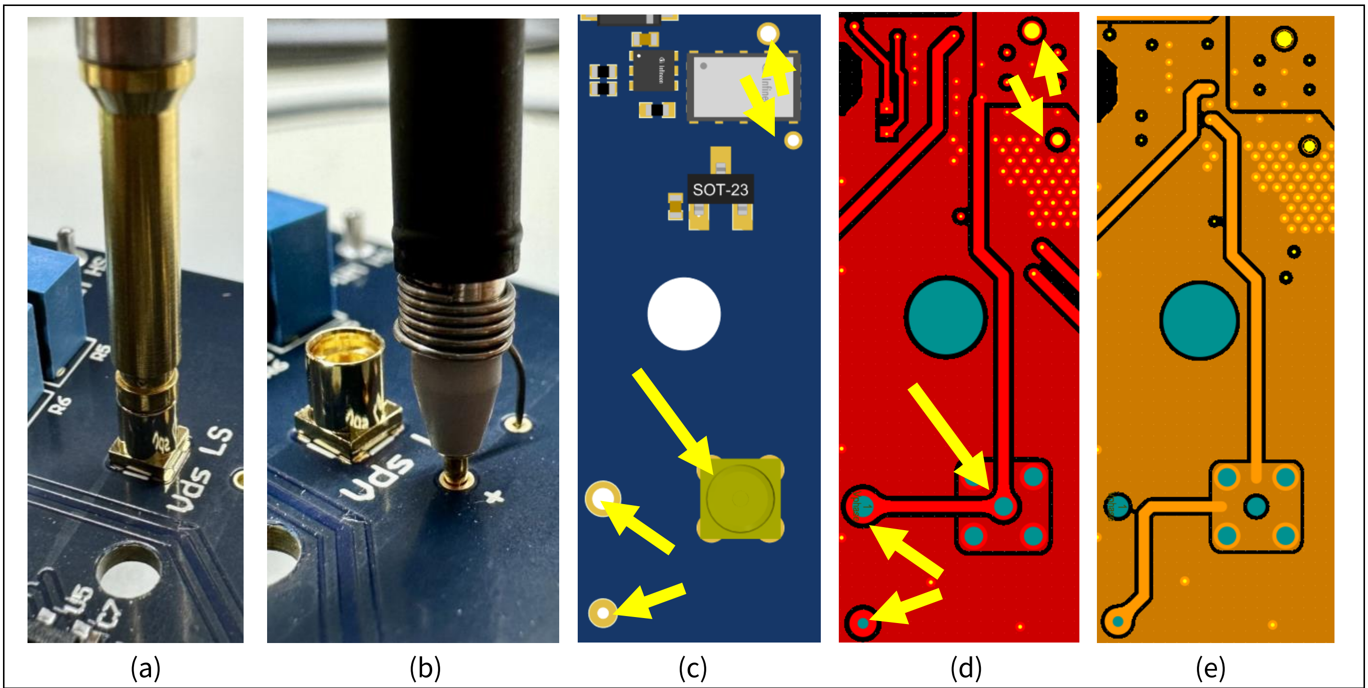


Figure 8 **Low-side VDS waveform probing techniques implemented in EVAL_7136U_100V_GaNc. (a) Probe attachment with MMCX tip, (b) probe attachment with spring-clip, (c) 3D view of measurement connection options, (d) Outer layer routing of drain voltage**

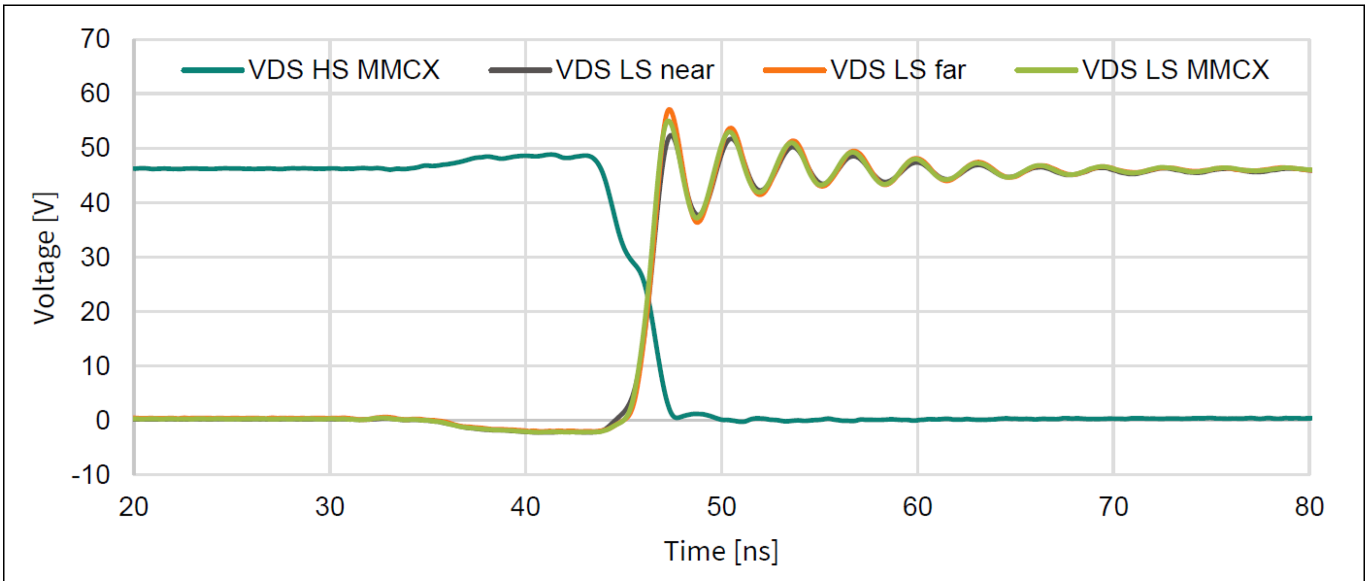


Figure 9 **Low-side VDS waveforms measured in the three location options on EVAL_7136U_100V_GaNc, when operated in a 48 V buck converter at 20 A output current, captured during a high-side turn-on transition**

2.4.2 Dead-time selection and induced turn-on risk assessment

This section proposes a technique for selecting dead-time based on the tradeoff between DLB conduction loss and the so-called "double hard-switching" explained in [14]. The same test sequence also helps to diagnose the design's risk of Miller-induced false turn-on, which may sometimes be mitigated with careful dead-time selection.

The first consideration in dead-time selection is the sum of all propagation delays in the PWM signal chain, which could lead to catastrophic shoot-through when the tolerance of all delays stack-up in the same direction. For example, the propagation delay for the microcontroller may be specified as 20 ns ± 2 ns. The GDIC may have a specified propagation delay of 30 ns ± 2 ns and rise/fall times of 5 ns ± 1 ns. This means that the total delay for turn-on or turn-off of either GaN transistor is typically 55 ns but it could be as short as 50 ns or at long as 60 ns.

If the controller's dead-time is programmed for 10 ns based on measurements with typical delays, then the actual dead-time could be 0 ns in an extreme case of tolerance stack-up, where the high-side has the longest possible turn-off delay (60 ns) and the low-side has the shortest possible turn-on delay (50 ns). The minimum dead-time based on propagation delay tolerances is reduced when a half-bridge GDIC specifies the exact timing skew between either turn-off and the complementary turn-on. Furthermore, the propagation delay tolerances of the controller can be ignored when the GDIC offers a local dead-time selection with a resistor option at one of its pins. In most cases, a dead-time in the range of 10-30 ns is a reasonable choice based on these considerations.

The proposed technique for dead-time selection involves repeating the same test condition over a range of dead-time values, to produce trend lines as shown in Figure 10. This example was run on motor drive evaluation board [10] at 48 V, 100 kHz, and three AC output currents. The minimum dead-time was selected as 16 ns in this case, based on the propagation delays involved and the 8 ns timing resolution of the controller. It is clear in this trend that the optimal dead-time for 10 A and 20 A_{PK} is the lowest one, 16 ns. However, the lowest current of 5 A_{PK} shows a slightly increased power loss at 16 ns compared to 32 ns. This extra loss is caused by partial hard-switching when the high-side transistor turns on at the end of the 16 ns dead-time before the lossless ZVS transition could complete. Figure 11 shows the waveforms for these two scenarios. The time required for a lossless ZVS transition is inversely proportional to load current so this behavior is most obvious at the lightest loads. In this example, the extra loss at light load is much lower than the savings at higher loads, so perhaps 16 ns is still the optimal dead-time selection. Other designs or applications may see a different tradeoff and favor a slightly longer dead-time as a consequence.

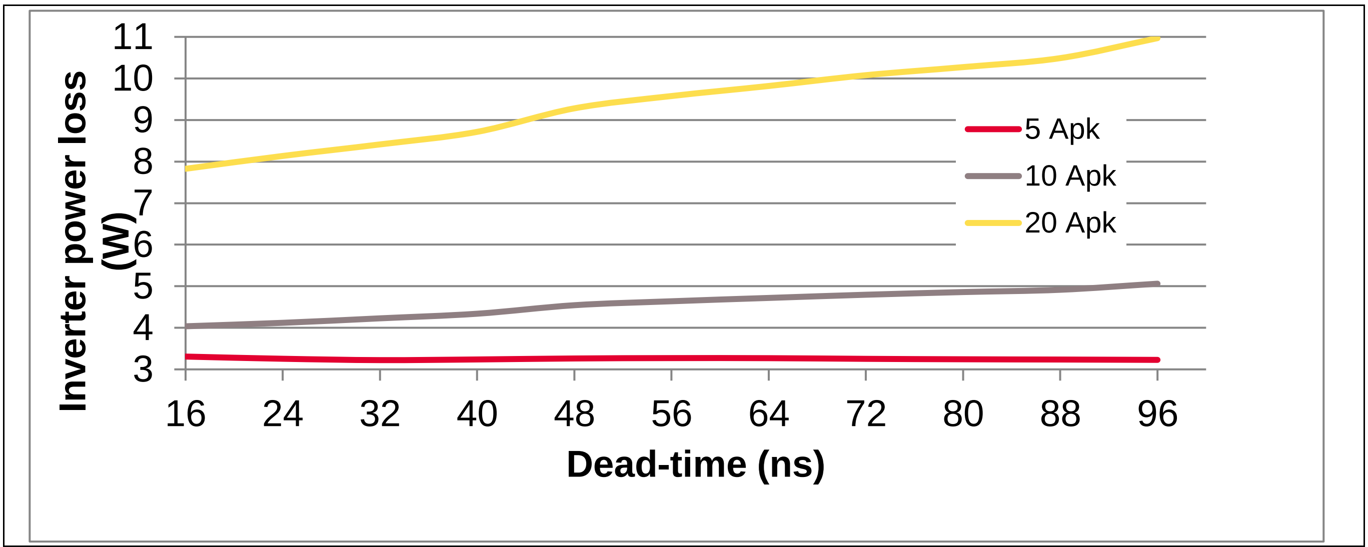


Figure 10 **Power loss of a 48 V motor drive, operating at 100 kHz and three AC load currents, in a parametric sweep of the dead-time**

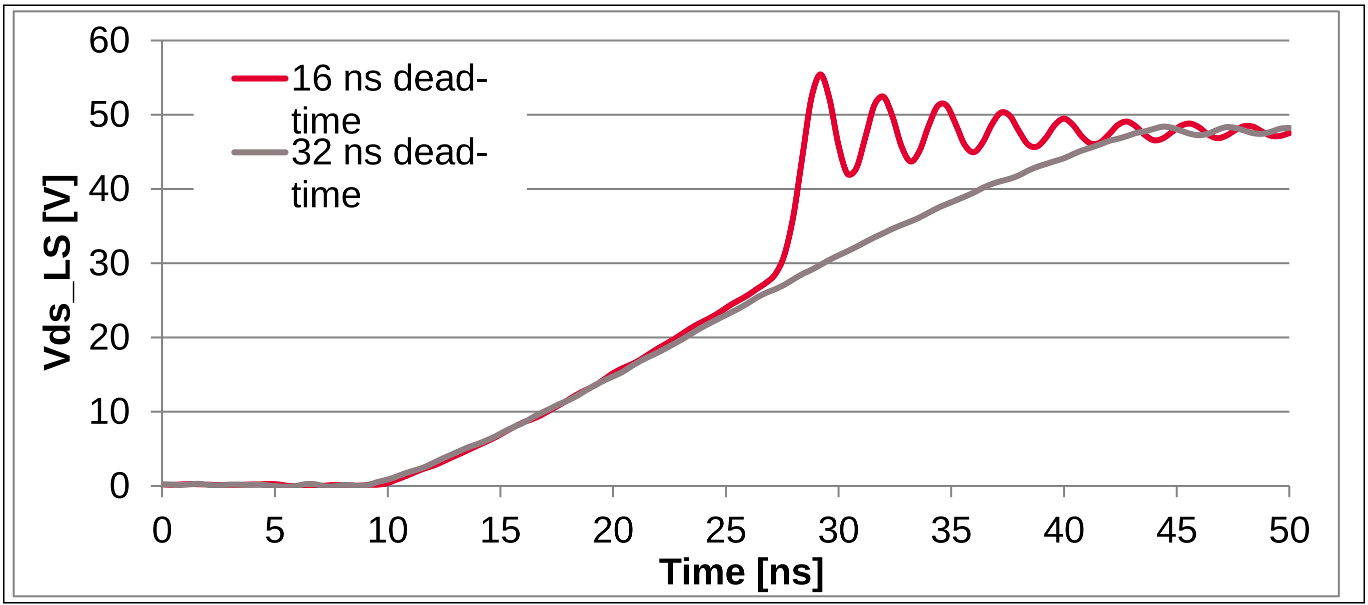


Figure 11 **Switching waveforms of a 48 V motor drive, operating at 100 kHz and 5 APK AC load current, demonstrating the partial hard-switching that can occur at low currents when a short dead-time is used, rather than the lossless ZVS transition with a longer dead-time**

This test methodology has a secondary outcome, which helps to diagnose the risk of Miller-induced false turn-on. When one transistor in a half-bridge experiences a hard turn-on transition, the Miller effect causes a positive excursion of the complementary transistor's gate voltage. This mechanism can lead to additional power loss from partial shoot-through in each switching transition or even to catastrophic shoot-through events in extreme cases. A strong pull-down from the GDIC limits this risk, especially in the form of an active Miller clamp, but this pull-down may be bottlenecked by added gate resistance or parasitic inductance in the turn-off gate loop. It is difficult to diagnose this phenomenon in a GaN half-bridge, as it may not cause obvious distortions in switching waveforms [15], Figure 12 and Figure 13 show this phenomena.

As visible on Figure 12 around 7 to 20 ns, there is a glitch in the power losses compared the more linear behavior at different dead-times. This is happening in the case of a not-well optimize gate driving loop, where the parasitic inductance located in the gate loop of the low side, is preventing the driver to keep the low side GaN off during the fast transition between OFF and ON of the high-side.

Figure 12 emphasize that meanwhile the voltage on the low side gate shows a high glitch, the effect on the drain-source measurements of the low-side GaN are almost invisible.

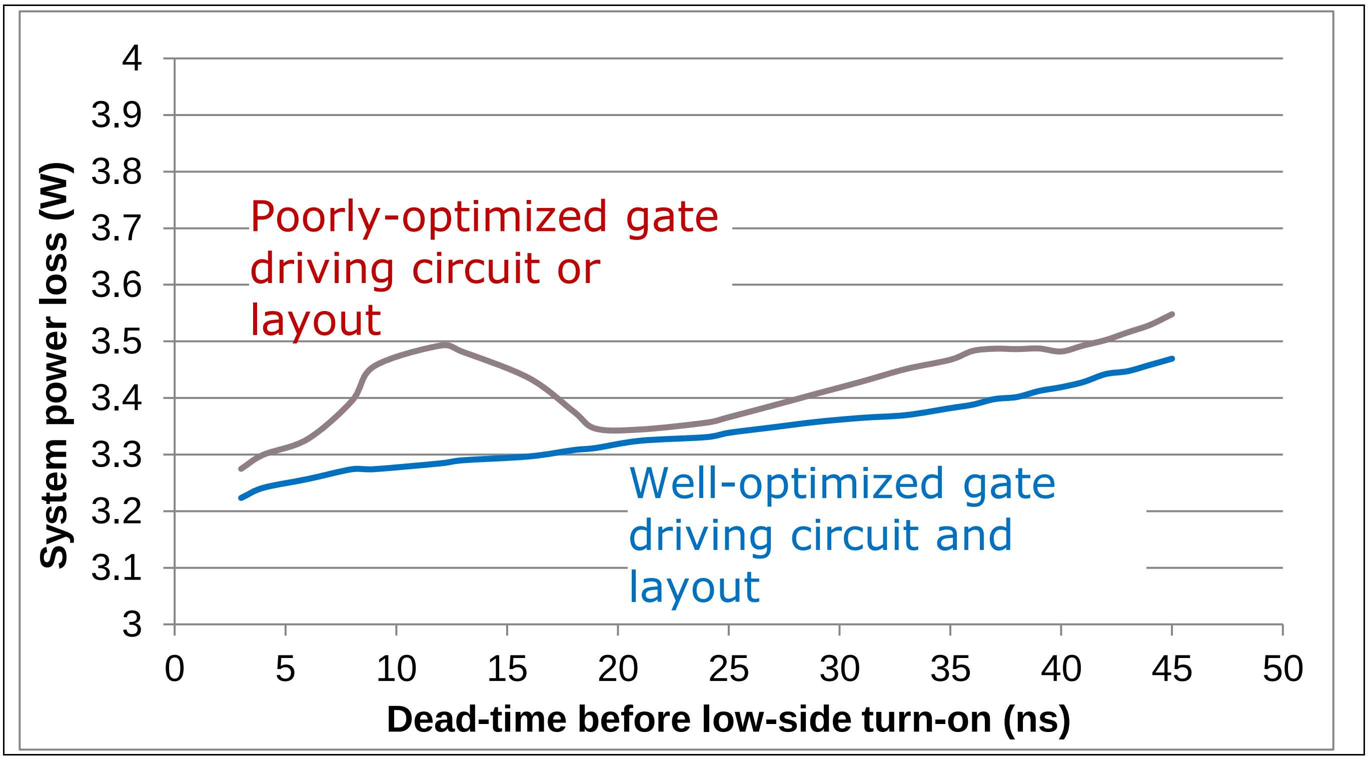


Figure 12 **Power loss of a 48 V to 12 V buck converter, operating at 400 kHz and 10 A output, in a parametric sweep of the dead-time before low-side turn-on**

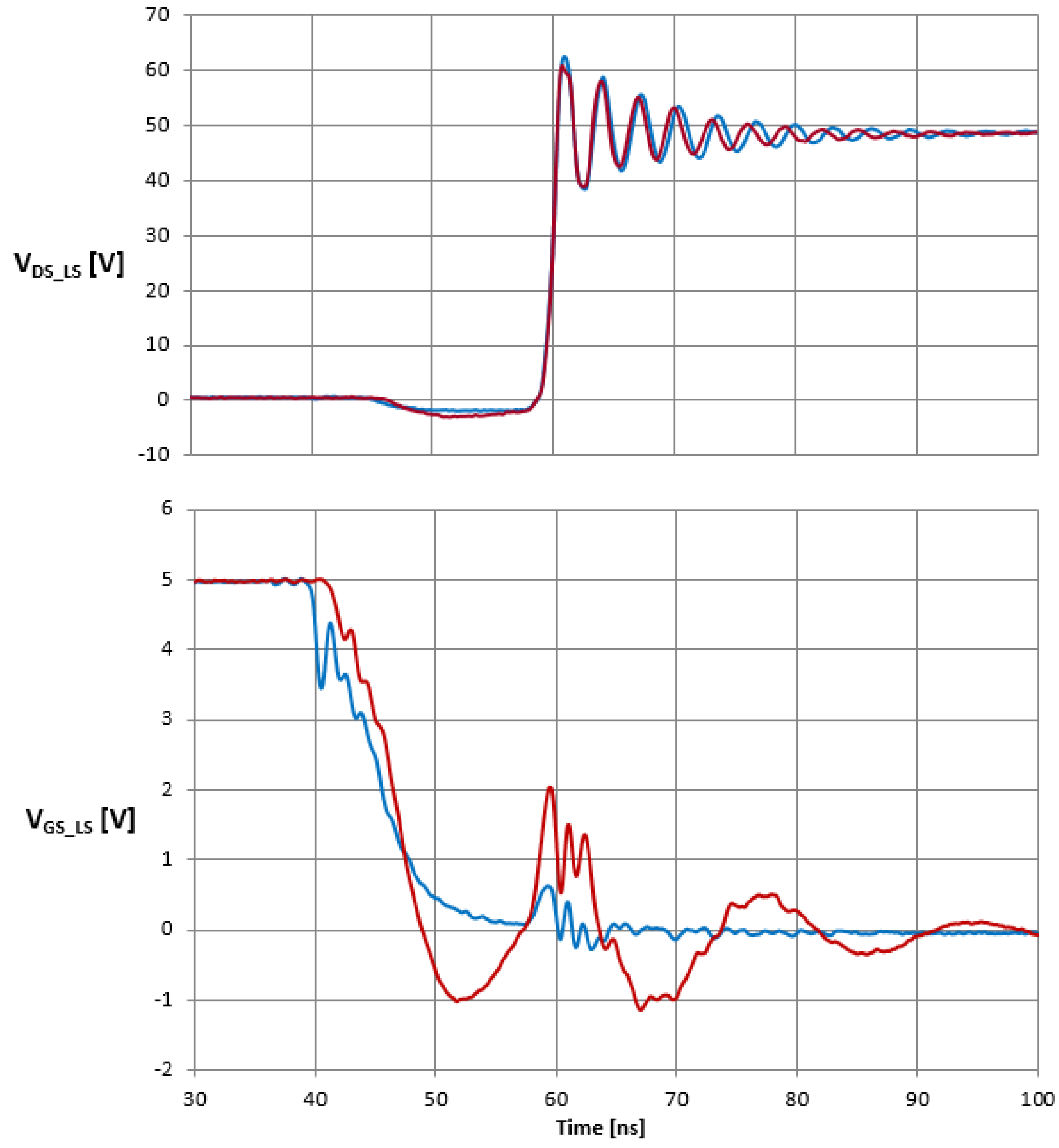


Figure 13 **Switching waveforms of a 48 V to 12 V buck converter, operating at 400 kHz and 10 A output, in a parametric sweep of the dead-time before low-side turn-on. Comparison shows a well-optimized gate driving circuit/layout vs. a poorly-optimized gate driving circuit/layout at 12 ns dead-time**

3 Summary

This application note depicts a short introduction on GaN HEMT technology and the driving circuit implementation. The core part of the application note is addressing the key aspects of the layout for a half-bridge GaN with driver.

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