Application Note

# Astra™ Machina Foundation Series eMMC Configuration

Abstract: This application note provides detailed guidelines for connecting and configuring the eMMC with the SL1620, SL1640, SL1680 and SL2610 RDK.

# Contents

# List of Figures

# List of Tables

# 1. Overview

The Astra Machina RDK (Reference Development Kit) is a versatile development platform for embedded system applications. It is equipped with a high-performance processor and a suite of peripherals to accelerate system prototyping and development. This application note provides detailed guidance on integrating and using an eMMC device with the Astra Machina RDK platform.

## 1.1. Scope

This document is intended for developers using the Astra Machina RDK platform to prototype systems that require eMMC for storage and boot. It provides detailed design recommendations, hardware design, and troubleshooting tips to ensure proper eMMC operation.


*Figure 1. Overview of Astra Machina Foundation Series*



The Astra Machina RDK platform supports an integrated eMMC controller compliant with JEDEC eMMC 5.1 specifications. Summary of eMMC Speed Modes:

*Table 1. eMMC Speed Modes supported by Astra Machina RDK*

| Mode | Bus Speed | Bus Widths | Clock Frequency | I/O Voltage |
|---|---|---|---|---|
| Legacy Mode | 25MB/s | 1-bit, 4-bit, 8-bit | 25MHz | 1.8V |
| High-Speed | 50MB/s | 1-bit, 4-bit, 8-bit | 50MHz | 1.8V |
| DDR52 | 100MB/s | 4-bit, 8-bit | 50MHz | 1.8V |
| HS200 (SDR) | 200MB/s | 4-bit, 8-bit | 200MHz | 1.8V |
| HS400 (DDR) | 400MB/s | 8-bit | 200MHz | 1.8V |

## 1.2. Hardware Connection of eMMC on Astra RDK

### 1.2.1. Power supply of eMMC

The Astra Machina series SoC supports a fixed 1.8V I/O signaling voltage for eMMC. The eMMC power supply requirements.

*Table 2. eMMC pin assignment with Voltage*

| Name | Voltage | Description |
|---|---|---|
| VCC | 3.3V | Power supply for EMMC CORE |
| VCCQ | 1.8V | Power supply for I/O |

### 1.2.2. Resistors/Capacitor on eMMC Bus

- **Pull-Up resistors:** The SL16x0 eMMC controller includes internal pull-up resistors for the CMD and DATA[7:0] signals. Therefore, no external pull-up resistors are required.
- **Pull-Down resistors:**
  - Connect the eMMC RSTn signal to GND through a 4.7 kΩ resistor.
  - Connect the eMMC STRB signal to GND through a 47 kΩ resistor.
- **Series resistors:**
  - Place a 22 Ω or 33 Ω series resistor on the eMMC CLK and eMMC STRB signals.
  - Series resistors are not required on other eMMC signals.
- **Capacitor:** Place a 0.1 µF capacitor on the eMMC RSTn pin

### 1.2.3. VDDI Capacitor

To prevent voltage fluctuations on the **VDDI** pin, it is recommended to place a combination of **4.7 µF** and **0.1 µF** decoupling capacitors in parallel.



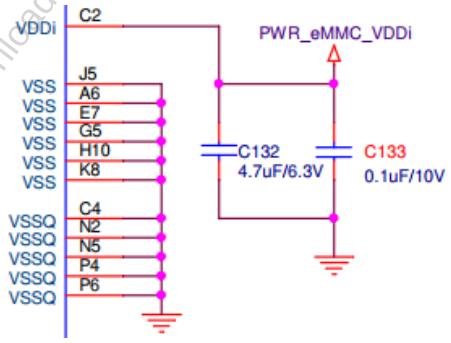


*Figure 2. Capacitors on VDDI*

## 1.3. eMMC Boot mode

The Astra Machina RDK platform is typically designed to support **eMMC Boot Mode** as defined by the JEDEC eMMC standard. Boot mode allows the system to directly load the bootloader (or firmware) from the eMMC's boot partitions, making it a common and reliable method for embedded system initialization.

To boot from the eMMC device, both the Astra Machina **processor** and the **eMMC device** must be properly configured in **eMMC Boot Mode**.

- SL16x0 Boot Strap pin: Configure Boot_SRC[1:0] pins to 2'b10 for eMMC Boot mode.

| BootSrc[1:0] | TYPE |
|---|---|
| 2'b00 | SPI-Secure Boot |
| 2'b01 | ROM boot from NAND default |
| 2'b10 | ROM boot from EMMC |
| 2'b11 | SPI-Clear Boot |

- SL261x Boot Strap pin: Configure Boot_SRC[1:0] pins to 2'b10 for eMMC Boot mode too.

| BootSrc[1:0] | TYPE |
|---|---|
| 2'b00 | ROM boot from USB2 |
| 2'b01 | ROM boot from xSPI_NOR |
| 2'b10 | ROM boot from EMMC default |
| 2'b11 | ROM boot from xSPI_NAND |

*Figure 3. Boot mode of Astra Machina processor*



- eMMC EXT_CSD register:
  - EXT_CSD[177] for Boot partition config.
  - EXT_CSD[179] for Bus Width and Speed Mode config.
  - For more information, see JESD84-B51.

## 1.4. Internal Pull-Up resistors Control

The **eMMC controller** of the **SL16x0 SoC** includes built-in internal pull-up resistors for the eMMC bus signals. The configuration and control of these resistors can be managed using the registers listed in Table 3.

*Table 3. eMMC Internal Pull-Up/Dn resistor register*

| Name | Register Address | Description | Recommended Value |
|---|---|---|---|
| CMDPAD_CNFG | 0x304[4:3] | • 0x0 (DISABLED): Pull-up and pull-down functionality disabled<br>• 0x1 (PULLUP): Weak pull up enabled<br>• 0x2 (PULLDOWN): Weak pull down enabled<br>• 0x3 (ILLEGAL): Should not be used | 0x1 |
| DATPAD_CNFG | 0x306[4:3] | | 0x1 |
| CLKPAD_CNFG | 0x308[4:3] | | 0x0 |
| STBPAD_CNFG | 0x30A[4:3] | | 0x2 |

**Note:** SL16x0: EMMC_REG_BASE is 0xF7AA0000, SL261x: EMMC_REG_BASE is 0xF7A00000.



## 1.5. Delay-Line Tuning

The **eMMC controller** of the **Astra Machina SoC** supports the **Tuning Function** for both **Read** and **Write** operations. This ensures reliable high-speed data transfers in modes such as **HS200** and **HS400** by calibrating the signal timing for optimal performance.

### *1.5.1. Read Tuning*

In **HS200** and **HS400** modes, the host adjusts the **sampling point** to reliably receive data. During initialization, the host sends **CMD21** (Tuning Command) to the eMMC device, which responds with a tuning pattern. The host performs the tuning sequence to find the optimal sampling point, ensuring reliable high-speed communication.

### *1.5.2. Write Tuning*

The Astra Machina processor provides an eMMC_CLK TX Delay Line Adjustment function for all speed modes. This feature ensures optimal timing alignment for high-performance eMMC operation.

The register in Table 4 is used to configure the eMMC_CLK TXDLY.

*Table 4. eMMC CLK TXDLY register*

| Name | Register Address | Description |
|---|---|---|
| SDCLKDL_DC | 0x31E[6:0] | Drives eMMC CLK DelayLine's Delay Code input. |

**Note:** SL16x0: EMMC_REG_BASE is 0xF7AA0000, SL261x: EMMC_REG_BASE is 0xF7A00000.

  

Table 5 lists the recommended **TXDLY** settings for the **eMMC_CLK** signal based on the speed mode.

*Table 5. eMMC CLK TXDLY Recommended Setting*

| Board | eMMC Speed Mode | | | | | |
|---|---|---|---|---|---|---|
| | Identical | Legacy | HS-SDR | HS-DDR | HS200 | HS400 |
| SL1680_RDK | 40 | 40 | 40 | 40 | 40 | 20 |
| SL1640_RDK | 40 | 40 | 40 | 40 | 40 | 20 |
| SL1620_RDK | 40 | 40 | 40 | 40 | 40 | 20 |
| SL261x_RDK | 40 | 40 | 40 | 40 | 40 | 20 |

## 1.6. PCB Layout Guidelines

- Minimize the length of the CLK, CMD, and DAT traces to reduce signal latency and interference.
- Use controlled impedance routing for high-speed signals (CLK, CMD), typically 50ohm Single-End.
- Match trace lengths for CLK, CMD, DAT0-DAT7 to ensure proper signal timing in high-speed modes.
- Avoid crossing noisy components (e.g., switching power regulators) with high-speed signal traces.

# 2. References

- *Astra Machina™ Foundation Series Quick Start Guide* (PN: 511-001404-01)
- *SL1620 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001428-01)
- *SL1640 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001415-01)
- *SL1680 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001413-01)
- *SL2610 Product Line of Embedded Processor Datasheet* (PN: 505-001501-01)
- Embedded Multi-Media Card (eMMC) Electrical Standard (5.1) (JESD84-B51)

# 3. Revision History

| Revision | Description |
|---|---|
| A | Initial release. |
| B | Minor update to correct trademarked items.. |
| C | Minor update to trademarked items. |
| D | Added eMMC for SL2610. |





**Contact Us**

Visit our website at www.synaptics.com to locate the Synaptics office nearest you.

PN: 506-001594-01 Rev D